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APPLICATION

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TITLE: REDUCING LEAKAGE CURRENTS IN MEMORIES WITH PHASE-CHANGE MATERIAL

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REDUCING LEAKAGE CURRENTS IN MEMORIES WITH PHASE-CHANGE MATERIAL

Background

This invention relates generally to memories that use phase-change materials.

Phase-change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure and the crystalline state involves a more ordered atomic structure. Generally, any phase-change material may be utilized; however, in some embodiments, thin-film chalcogenide alloy materials may be particularly suitable.

The phase-change may be induced reversibly. Therefore, the memory may change from the amorphous to the crystalline state and may revert back to the amorphous state thereafter or vice versa. In effect, each memory cell may be thought of as a programmable resistor, which reversibly changes between higher and lower resistance states.

In some situations, the cell may have a large number of states. That is, because each state may be distinguished by its resistance, a number of resistance determined states may be possible allowing the storage of multiple bits of data in a single cell.

A variety of phase-change alloys are known. Generally, chalcogenide alloys contain one or more elements from column VI of the periodic table. One particularly suitable group of alloys are GeSbTe alloys.

A phase-change material may be formed within a passage or pore defined through a dielectric material. A phase-change material may be sandwiched between lower and upper electrodes.

A buried wordline structure may be utilized to provide signals to the lower electrode of a phase-change material memory cell. These signals may include programming signals to change the programming state of the cell or read signals to read the current state of the phase-change material.

A buried wordline may form a diode in a substrate under the lower electrode. The diode necessarily has a certain reverse bias leakage current to the substrate. In particular, the diode is formed of a P+ layer over an N+ layer over a P type substrate. When the N+ type layer is reverse biased between the N type layer and the substrate, an N+/N-/P- diode is formed whose reverse leakage current may be substantial.

Generally, the N+ layer must be relatively narrow resulting in higher wordline resistance. These structures may have relatively high resistance and at times may have substantial leakage currents.

Thus, there is a need for way to reduce the leakage currents of phase-change memory cells.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of a phase-change memory cell in accordance with one embodiment of the present invention;

Figure 2 is a cross-sectional view of the embodiment shown in Figure 1 at an early fabrication stage;

Figure 3 is a cross-sectional view of the embodiment shown in Figure 2 after further processing in accordance with one embodiment of the present invention;

Figure 4 is a cross-sectional view of the embodiment shown in Figure 3 after still further processing in accordance with one embodiment of the present invention; and

Figure 5 is a schematic depiction of a processor-based system in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a phase-change memory cell 10 may include a phase-change material 32 formed in a pore 24.

The pore 24 may include an etched aperture formed through a dielectric material 30. In some embodiments, the walls of the dielectric material 30 and the pore 24 may be defined by a cylindrically shaped sidewall spacer 36. Thus, in some embodiments, the phase-change material 32 may coat the walls of the pore 24 defined by the sidewall spacer 36 and may come in contact with the lower electrode 18. An upper electrode 34 may be defined over the phase-change material 32.

Signals may be applied through the lower electrode 18 to the phase-change material 32 and on to the upper electrode 34. These signals may include set and reset signals to change the programmed state of the phase-change material 32 as well as read signals to read the programmed state.

The signals are supplied to the lower electrode 18 through a buried wordline 22 in one embodiment. In accordance with one embodiment of the present invention, the buried wordline 22 includes a more lightly doped or an N- region 22a over a more heavily doped or N+ region 22b over a more lightly doped or N- region 22c. The substrate 12 may be more lightly doped or P- material and layer 20 may be more heavily doped or P+ material.

In accordance with some embodiments of the present invention, the configuration of the buried wordline 22 reduces leakage current under reverse bias conditions,

thereby lowering the standby current needed for the memory cells 10. The lower buried wordline resistance may result in less voltage drop along the row lines, enhancing the programming operation efficiency and lowering the programming current in some embodiments. In addition, the resulting diode, made up of the layers 20 and 22, may have an increased Zener breakdown voltage.

Turning next to Figure 2, the formation of the memory cell 10 may begin by forming a pair of spaced trenches 16 in the substrate 12. The trenches 16 may isolate one wordline from adjacent wordlines that make up a memory array. The trenches 16 may be filled with an oxide 14 in some embodiments. The region between the trenches 16 may then be subjected to a series of ion-implantation steps, indicated at I.

As a result of a sequence ion-implantation steps, a diode formed of a P+ region 20 over an N type buried wordline 22 may be defined in a P- substrate 12. In particular, the energy, dose and doping profiles of a series of implants may be adjusted to achieve the sequence of layers 22a, 22b and 22c indicated in Figure 3. That is, the concentration profile resulting from a plurality of implants may be selected so as to create the specied series of doped layers 22 by adjusting the depth of each implant's concentration profile.

While the exact nature of the ion-plantation steps may be subject to considerable variation, an initial implantation may be utilized to form a P type well. This may be followed by a P type and N type implant to form the buried wordline 22 and overlaying P+ region 20. These implants in turn may be followed by one or more additional implants, in some embodiments, to create the profiles indicated in Figure 3. In some embodiments, the P type region may be formed by a boron implant and the N type region may be formed by a phosphorus implant.

Through the provision of the N- regions 22a and 22c, the reverse bias leakage current of the resulting cell 10 may be significantly improved in some embodiments. The implanted layers may be subjected to sufficient heat processing to achieve the desired performance.

A lower electrode layer 18 may be formed over the layers 20 and 22 as shown in Figure 4. In some embodiments, the lower electrode 18 may be formed of cobalt silicide. Thereafter, the cell 10 may be completed by defining the pore 24 and developing the structure shown in Figure 1. Of course any of a variety of cell structures may be utilized in accordance with embodiments of the present invention.

Referring to Figure 5, the memory cell 10 shown in Figure 1 may be replicated to form a memory array including a large number of cells. That memory array may be utilized

as the memory of a wide variety of processor-based systems such as the system 40 shown in Figure 5. For example, the memory array may be utilized as the system memory or other memory in a variety of personal computer products such as laptop products, desktop products or servers. Similarly, the memory array may be utilized in a variety of processor-based appliances. Likewise, it may be used as memory in processor-based telephones including cellular telephones.

In general, the use of the phase-change memory may be advantageous in a number of embodiments in terms of lower cost and/or better performance. Referring to Figure 5, the memory 48, formed according to the principles described herein, may act as a system memory. The memory 48 may be coupled to a interface 44, for instance, which in turn is coupled between a processor 42, a display 46 and a bus 50. The bus 50 in such an embodiment is coupled to an interface 52 that in turn is coupled to another bus 54.

The bus 54 may be coupled to a basic input/output system (BIOS) memory 62 and to a serial input/output (SIO) device 56. The device 56 may be coupled to a mouse 58 and a keyboard 60, for example. Of course, the architecture shown in Figure 5 is only an example of a potential architecture that may include the memory 48 using the phase-change material.

While the present invention has been described with respect to a limited number of embodiments, those skilled

in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: